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DESIGN AND IMPLEMENTATION OF MMIC BASED LOW NOISE AMPLIFIER CIRCUITRY FOR PASSIVE PROGRAMMABLE STIMULATOR IMPLANTS

Rinju Pappachan Jagadeesh Kumar P[1]

Abstract-Programmable stimulator implant generates different types of stimulation patterns for different organs. A passive implant can derive power from the wireless power transfer at radio frequency. Signals received by the antenna in wireless systems are very weak. A low noise amplifier is needed to amplify the weak signal received by the antenna with minimum self-generated noise. LNA's are usually used as the front end of a receiver system. It is usually located at the focal point on the antenna, so that it can receive and amplify the weak signals thereby can overcome the system losses of the receiver. The LNA must have the lowest noise, so it doesn't add noise to the microwave system. Size of LNA should be very low since it is for medical implants. CMOS MMIC (micro monolithic integrated circuit) LNA is presented in this work.

1. INTRODUCTION

In a programmable stimulator implants the signal re-ceived by the antenna is very weak. A low noise amplifier is needed to amplify the signal with minimum self-gener-ated noise.

CMOS devices are typically used in low-noise amplifiers in the microwave frequency region. Low power consumption, low cost and easy availability were the main reasons to choose the CMOS process. The use of Monolithic Microwave Integrated Circuit component technology in modern microwave systems is be-coming more and more important. The main reason for this is the ability to achieve small size and weight. It also has advantages in terms of reliability, repeatability of performance and reduction of parasitic. However, the foundry cost is very high and design duration can take three to six months. This makes the pre-manufacturing cost expensive.

Implanted medical devices can be classified into active and passive based on the source of power. Active implants use a battery as the power source but have less implant ability. Whereas a passive implant can derive power from the wireless power transfer at RF. Such implants have restrictions on the amount of power available to them but have great implant ability. Passive implants have less area compared to active implants.

LNA should have a suitable gain (greater than 10dB) and an ultra-low noise figure at a supply voltage of 1V, such that it consumes very low power. It should be stable over the frequency range of 1.7 to 1.9 GHz. The characteristic impedance is chosen as 50. The LNA can be used for a programmable passive implant as the design is optimized for low power, low noise and less size.

2. RELATED WORKS

The need for a Low Noise Amplifier in Wireless im-plants has become a lot more sophisticated as these sys-tems has become mature and more widespread. LNA should minimize the noise figure, provide good input matching, and should have a sufficient gain. Radio Fre-quency (RF) low noise amplifiers have been designed to operate over a range of RF frequencies. In most of the designs, minimizing the noise figure with sufficient gain is given priority. Power consumption is also an important parameter.

Size of LNA is a design constrained because it is de-signed for an implant. So MMIC technology is used. MMICs were originally fabricated using gallium arsenide (GaAs), a III-V compound semiconductor. It has two fun-damental advantages over Silicon (Si), the traditional ma-terial for IC realization: device (transistor) speed and a semi-insulating substrate. Both factors help with the de-sign of high frequency circuit functions. However, the speed of Si-based technologies has gradually increased as transistor feature sizes have reduced and MMICs can now also be fabricated in Si technology. The primary advan-tage of Si technology is its lower fabrication cost com-pared with GaAs. Silicon wafer diameters are larger (typ-ically 8" or 12" compared with 4" or 6" for GaAs) and the wafer costs are lower, contributing to a less expen-sive IC. Indium Phosphide (InP), have been shown to of-fer superior performance to GaAs in terms of gain, higher cut off frequency, and low noise. However, they also tend to be more expensive due to smaller wafer sizes and in-creased material fragility. Silicon Germanium (SiGe) is a Si-based compound semiconductor technology offering higher speed transistors than conventional Si devices but with similar cost advantages. Gallium Nitride (GaN) is also an option for MMICs. Because GaN transistors can operate at much higher temperatures and work at much higher voltages than GaAs transistors, they make ideal power amplifiers at microwave frequencies.[12]

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[1] Asst.Prof., Department of Electronics Engineering, Model Engineering College, Thrikkakara

In the last decade, a great effort has been spent by academic and industrial research to investigate the poten-tial of GaN based active devices to realize LNAs. The inherent high linearity and power-handling capabilities of GaN HEMTs could represent a stunning advance to-ward the possibility of fabricating extremely robust and linear LNAs. Several researches on GaN-based LNAs were reported in open literature, both in hybrid and mono-lithic technologies, showing that a high maturity level was reached for applications at least up to Ku-band. In partic-ular, S-, C-, and X-bands are the most targeted frequency ranges because of their historical use for telecommunica-tions, radar, and electronic warfare [2]. As far as hybrid technology is concerned, operating frequencies are nar-rowed down to 3 GHz . In [15], exploiting a GaN HEMT power bar, an extremely high output IP3 of 54 dBm at 2 GHz was demonstrated with 2 dB associated noise figure. Also in [9],the circuit was based on a GaN HEMT power bar, directly bonded into a hybrid microstrip circuit, and the LNA design was oriented toward obtaining an output IP3 over 49 dBm while achieving 15-dB gain and a noise figure not >2 dB at 1.8 GHz. The two-stage GaN HEMT hybrid LNA proposed in [15] was designed to operate up to 3 GHz and to achieve up to 42-dBm output IP3 together with over 12-dB gain and <1.6-dB noise figure. Moving to monolithic technology, and focusing again on linearity as one of the main figures of merit for LNA design, [3] recorded over 51-dBm output IP3 and <3-dB noise figure measured at 2 GHz for an MMIC cascode feedback LNA. Other interesting results were reported in [4], where two MMIC single-stage LNAs, operating at 7 GHz, are fea-tured by over 43-dBm output IP3.
The combination of high peak electron velocity, high electron concentration and low band gap (0.36 eV) in the channel makes InAs/AlSb based high electron mobility transistor (HEMT) a promising device candidate for mi-crowave/ millimeterwave circuits operating at very low power consumption. High-gain and low-noise circuits based on the InAs/AlSb HEMT technology and operat-ing at dc power consumption below 10 mW have been reported. Recent publications have demonstrated that, at 77 K, the InAs/AlSb HEMT shows large improvements in terms of gate leakage current, transconductance, gain and noise figure. [5]
GaAs FET devices are typically used in low-noise am-plifiers in the microwave frequency region where silicon transistors can't provide the required gain and noise per-formance. There are, however, many applications in the frequency range below 2 GHz where the low noise figures and high gain of GaAs FETs can improve receiver sensi-tivity. Typical applications include low noise amplifiers (LNAs) in the 800 to 900 MHz frequency range for use in cellular telephone and pager applications and spread spec-trum transceiver applications.
CMOS is the only device which works in 1V supply. The above studied materials will not work in that sup-ply voltage. And hence a comparative study of different CMOS technology is performed.
The frequency of an RF electromagnetic wave can be important in determining how much energy is absorbed and therefore, the potential for harm. The quantity used to characterize this absorption is called "specific absorption rate" or "SAR". SAR is a measure of the rate of RF energy absorption by the body from the source being measured. SAR provides a straight forward means for

Technology	W/L	Vdd (V)	Idss(nMOS) (uA)	Idss(pMOS) (uA)	Vth(nMOS) (V)	Vth(pMOS) (V)
180nm	.24/.18	1.2/2.5/ 3.3	565	-270	.45	-.43
130nm	.16/.12	1.2-1.5	457	-193	.41	-.42
90nm	.12/.10	1-1.2	526	-235	.53	-.44
65nm	.12/.06	.9-1.26	524	-245	.51	-.53

Figure 1: Comparison of various CMOS Technologies.

measuring the RF exposure characteristics of antennas to ensure that they are within the safety guidelines. SAR can also refer to absorption of other forms of energy by tissue, including ultrasound. It is defined as the power absorbed per mass of tissue. The unit of SAR is Watts per Kilogram (W/Kg). SAR is either averaged either over the whole body, or a small sample volume. Local SAR is determined over a mass of 10g.
At a particular frequency, the transmitted power is limited by tissue heating, which is measured by SAR and should not exceed 1.6mW/cm3 as averaged over any 1g of tissue according to the IEEE safety guidelines.
According to IEEE safety guidelines, SAR measures exposure to fields between 3KHz and 300GHz. The value will depend heavily on the geometry of the part of the body that is exposed to the RF energy, and on the exact location and geometry of the RF source.
S. Kim et. al. in Ref [6] explained the wireless power transfer between a source and a weakly coupled implant on the heart. With proper system design, power suffi-cient to operate typical cardiac implants can be received by millimeter-sized coils. From the analysis, the maxi-mum efficiency occurs at about 1.7 GHz and is more than an order of magnitude greater than efficiency in the MHz range.

3. PROPOSED SYSTEM

Basically, designing an amplifier, the input and output matching network are considered to achieve the required stability, small signal gain, and bandwidth. Super high frequency amplifier is a typical active circuit used to amplify the amplitude of RF signal. An LNA is a design that minimizes the Noise Figure of the system by matching the device to its noise matching impedance, or Gamma optimum (opt). Gamma op-timum (opt) occurs at impedance where the noise of the device is terminated. All devices exhibit noise energy. To minimize this noise as seen from the output port, one must match the input load to the conjugate noise impedance of the device. Otherwise the noise will be reflected from the load to the device and

amplified. While this gives a minimum noise figure, it often results in slightly reduced gain as well as possibility increasing the potential instabil-ities.

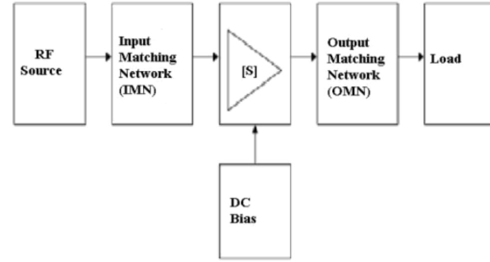
3.1 Block Diagram

Input to the LNA is from antenna, which is RF signal. The RF signal received by the antenna is needed to be amplified with minimum self-generated noise. There should be a matching between the RF source and the amplifier. And also the output of amplifier is matched with the circuit after that.

Figure 2: System Block Diagram.

3.2 Input Matching Network

The role of the input matching network is to make the input return loss (S11) minimized without introducing additional noise. The interface between the antenna and the LNA entails an interesting issue. Considering the LNA as a voltage amplifier, we may expect that the ideal value of its input impedance is infinite. From the noise point of view, we may require a



transformation network to precede the LNA so as to obtain minimum NF. From signal power point of view, we may utilize conjugate matching between the antenna and the LNA. The input matching network is designed by choosing the source impedance (Zs) equal to the optimum impedance (Zopt). In today's systems the LNA is designed to have a 50 ohm input impedance.

3.2.1 S parameter

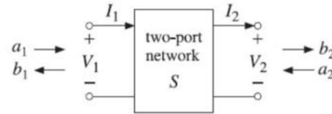


Figure 3: Two Port Network.[13]

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}, \quad S = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \quad \text{(scattering matrix)}$$

Figure 4: S parameter matrix.

The matrix elements S11, S12, S21, S22 are referred to as the scattering parameters or the S-parameters. The parameters S11, S22 have the meaning of reflection coef-ficients, and S21, S12, the meaning of transmission coef-ficients. Rollette's stability constant K is important to LNA de-sign. Stern Stability factor is defined in terms of s param-eter as:

$$K = \frac{1 + j\,4\,j^2 \quad jS11j^2 \quad jS22j^2}{2 \quad jS11j \quad jS22j} \qquad (1)$$

Where 4=S11S22-S12S21. If $K>1$ and $4<1$ then the circuit is unconditionally stable. Equation (3.1) suggests that stability improves as S12 decreases.

3.3 Amplifier Section

Amplifier section ensures a high gain, high linearity, low noise factor and low power consumption and at the same time it provides input impedance that can be conducive to the realization of broadband matching. The output buffer guarantees the output impedance is 50**Ω** in order to test.

3.4 Conjugate matching

The Figure 5 shows a general amplifier circuit with input and output matching circuits.

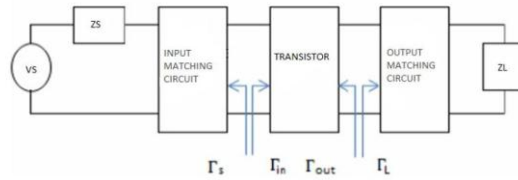


Figure 5: Basic transistor amplifier circuit with in-put and output matching networks.

The output matching network is designed by conjugate matching. Conjugate matched condition means that the reflection coefficient of the source ($_S$) is equal to the conjugate of the input reflection coefficient, $_{in}$ and the reflection coefficient of the load ($_L$) is equal to the conjugate of the output reflection coefficient, $_{out}$. This is for maximizing the transducer power gain. i.e. $_S$ = $_{in}$ and $_L$ = $_{out}$, where

$$_{in} = \frac{b1 = S_{11} + S21S12L}{a11\ S_{22}\ _{L}} \qquad (2)$$

$$out = \frac{b_2 = S_{22} + S21S12\ S}{a_2 1\ \ S_{11}\ _{S}} \qquad (3)$$

3.5 MMIC Technology

The use of Monolithic Microwave Integrated Circuit com-ponent technology in modern microwave systems is be-coming more and more important. The main reason for this is the ability to achieve small size and weight. It also has advantages in terms of reliability, repeatability of performance and reduction of parasitics. However, the foundry cost is very high and design duration can take three to six months. This makes the pre-manufacturing cost expensive. Moreover, post-fabrication tuning is prac-tically impossible. There are three basic points that should help in order to achieve this goal:

1. A reproducible / stable foundry process.
2. The foundry must provide accurate component mod-els, both active and passive.
3. The use of appropriate design methods.

Factors should be covered about the foundry process are cost of the foundry process, reputation, device perfor-mance, process stability, availability of active and passive structure models

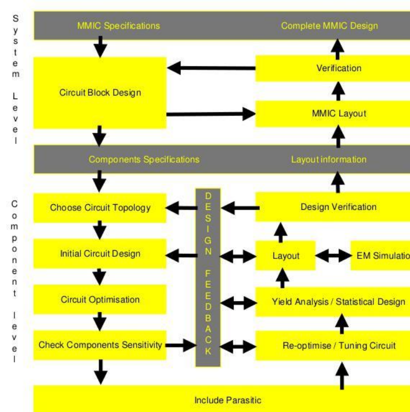


Figure 6: MMIC Design flow chart.[16]

The design cycle can be summarised by the flow chart shown. Work starts with circuit block design based on MMIC specifications and proceeds through circuit de-sign, optimisation and sensitivity and yield analysis to MMIC layout. The process is iterative, as shown. In an MMIC amplifier design select an active device with required specifications such as frequency, noise figure, gain etc. Then choose a bias point to maximize the transconductance gm. Impedance matching with ideal elements is needed. For this determine the optimal source and load reflection coefficient based on NF and gain. Add feedback elements between the terminals.

4. IRCUIT ANALYSIS AND DESIGN

4.1 Cascode Low Noise Amplifier with source degeneration

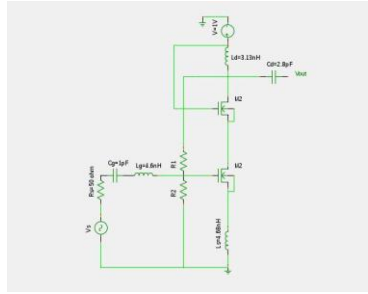


Figure 7: Cascode LNA with source degeneration.

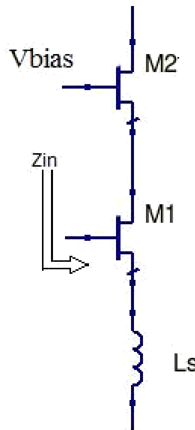
4.2 Analysis of Cascode stage with source degeneration

Figure 8 shows the input impedance, Zin of the cascade configuration of the Low Noise Amplifier.

Figure 8: Input impedance of an inductively degenerated Cascode amplifier.

The input impedance of the Common Source stage is given by:

$$Z_{in} = \frac{s{:}(L_s + L_g) +1+gm1(L_s)}{s{:}C_{gs}\,Cgs} \tag{4}$$



where C_{gs} is the gate source parasitic capacitance, g_{m1} is the transconductance of the FET M_1. L_s contribute a real term to the input impedance through interaction with C_{gs} and g_{m1}. By choosing L_s to resonate with C_{gs}, the impedance will look real at frequencies near the input res-onance. At resonance input impedance is,

$$Z_{in} = \frac{50 = g_m(L_s)}{Cgs} \tag{5}$$

Transit frequency ($!_T$) is given by the equation,

$$!_T = \frac{2\ f_T = g_m}{Cgs} \tag{6}$$

The value of source inductance L_s at resonance can be calculated using the equation,

$$L_s = \frac{50}{2\ f_T} \tag{7}$$

At resonance,

1 (8)

$s{:}(L_s + L_g) + \frac{}{s{:}C_{gs}} = 0$

$L_s + L_g = \frac{1}{!^2{:}C_{gs}}$ (9)

$C_{gs} = 1*10^{-10}$ (10)

Output section at resonance,

$s{:}L_d = \frac{1}{s{:}C_d}$ (11)

4.3 Noise Analysis Of The Cascode Stage

In an RF receiver, the noise contributed by subsequent stages may be neglected if the first stage possess sufficient gain. The noise figure of the Low Noise Amplifier can be approximated using the equivalent circuit in Figure. Elements R1, and Rg represent losses due to inductor resistance and gate resistance, respectively.

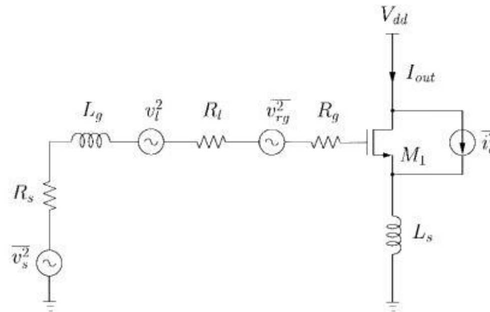


Figure 9: Equivalent circuit for input stage noise calculation.

The transconductance of the input stage is given by,

$$\begin{aligned} G_m &= g_{m1}Q_{in} = \frac{g_{m1}}{\omega_0 C_{gs}(R_s + \omega_T L_s)} \\ &= \frac{\omega_T}{\omega_0 R_s(1+\frac{\omega_T L_s}{R_s})} = \frac{\omega_T}{2\omega_0 R_s} \end{aligned} \quad (12)$$

where Qin, is the effective input Q of the circuit. Rl and Rg, have been neglected relative to Rs. The overall transconductance is apparently independent of gm, the intrinsic device transconductance. The noise figure of the circuit at resonance is given by,

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \gamma g_{d0} R_s \left(\frac{\omega_0}{\omega_T}\right)^2 \quad (13)$$

where Rg ,Rs and Rl are the gate, source, and input (in series with Cgs,) extrinsic ohmic resistances of the FET, respectively. Ro is the generator impedance, gm is the zero-bias drain conductance, !T is the unity current gain bandwidth and is a function of bias and is used to model channel noise for the FET. Rs and ri vary inversely with total device width, WT . Rs and ri substantially contribute to the noise figure.

Input Matching Network

The input matching network is designed using the optimum reflection coefficient opt. For noise matching,

$$\Gamma_s = \Gamma_{opt} \quad (14)$$

Output Matching Network

At the output side, conjugate matching is done. out is calculated using the equation,

$$\Gamma_L = \Gamma_{out}^* = \left(S_{22} + \frac{S_{21}S_{12}\Gamma_S}{1 - S_{11}\Gamma_S}\right)^* \quad (15)$$

By making use of smith chart, we can find out the input and output matching networks at a characteristic impedance of Zo = 50Ω.

5. CONCLUSION

The passive implants require a LNA with sufficient gain, contribute less noise and consumes as much less power as possible. A 90nm CMOS Cascode amplifier configuration is selected. Simulation is done using ANSOFT Designer .

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